REMARKS

Claims 1-56 are pending in this application. Paragraph [0006] of the specification has been amended to correct a typographical error.

Claims 1-8, 11, 13-24, 27, 29-43, 46, and 48-56 stand rejected under 35 U.S.C. § 103 as being unpatentable over Wang et al. (U.S. Patent No. 5,607,874) ("Wang") in view of Mizuhara et al. (U.S. Patent No. 6,228,438 B1) ("Mizuhara"). This rejection is respectfully traversed.

The claimed invention relates to a method of forming a composite barrier layer between a glass insulating layer and active regions of a memory device to eliminate the diffusion of impurity atoms from the glass insulating layer into the active regions of the device. As such, independent claim 1 recites a "method of forming a composite insulating structure" by *inter alia* "forming an oxide layer over at least said source/drain region . . . by oxidizing an upper surface of said source/drain region using atomic oxygen" and "forming a barrier layer over said oxide layer."

Independent claim 21 recites a "method for forming a memory cell" by *inter alia* "forming a composite barrier layer over said source/drain regions, said composite barrier layer comprising an oxide layer formed by oxidizing upper surfaces of said source/drain regions using atomic oxygen, and a barrier layer formed over said oxide layer." Similarly, independent claim 40 recites a "method of preventing the diffusion of atoms from a glass insulating layer in to a source/drain region formed between adjacent gate stacks of a memory device" by *inter alia* "forming a composite barrier layer over said source/drain regions, said composite barrier layer comprising an oxide layer formed by oxidizing upper surfaces of said source/drain regions using atomic oxygen, and a barrier layer formed over said oxide layer."

Wang relates to "a method for fabricating a T or Y shaped capacitor which has less photolithographic and etch steps than the conventional processes." (Col. 2, lines 28-

31). For this, Wang teaches the formation of several gate stacks over a substrate and of a source and drain region. (Col. 4). Wang also teaches the formation of an oxide layer (col. 5, lines 11-17) and of a barrier layer over source/drain regions. (Col. 5, lines 29-35).

Mizuhara relates to "a semiconductor device that allows the adhesion intensity between an upper insulation film and a lower insulation film to be improved." (Col. 2, lines 31-34). Mizuhara teaches the formation of "a silicon oxide film by CVD all over the device," which is a completed MOS transistor. (Col. 4, lines 50-53).

The subject matter of claims 1-8, 11, 13-24, 27, 29-43, 46 and 48-56 would not have been obvious over Wang in view of Mizuhara. Specifically, the Office Action fails to establish a *prima facie* case of obviousness. Courts have generally recognized that a showing of a prima facie case of obviousness necessitates three requirements: (i) some suggestion or motivation, either in the references themselves or in the knowledge of a person of ordinary skill in the art, to modify the reference or combine the reference teachings; (ii) a reasonable expectation of success; and (iii) the prior art references must teach or suggest all claim limitations. See e.g., In re Dembiczak, 175 F.3d 994, 50 U.S.P.Q.2d 1614 (Fed. Cir. 1999); In re Rouffet, 149 F.3d 1350, 1355, 47 U.S.P.Q.2d 1453, 1456 (Fed. Cir. 1998); Pro-Mold & Tool Co. v. Great Lakes Plastics, Inc., 75 F.3d 1568, 1573, 37 U.S.P.Q.2d 1626, 1630 (Fed. Cir. 1996).

Neither Wang nor Mizuhara, whether considered alone or in combination, teach or suggest the limitations of independent claims 1, 21 and 40. Neither Wang nor Mizuhara teaches or suggests "forming an oxide layer over at least said source/drain region . . . by oxidizing an upper surface of said source drain region using atomic oxygen," as independent claim 1 recites. Similarly, Wang and Mizuhara, whether considered alone or in combination, fail to teach or suggest "forming a composite barrier layer over said source/drain regions, said composite barrier layer comprising an oxide layer formed by oxidizing upper surfaces of said source/drain regions using atomic oxygen, and a barrier layer formed over said oxide layer," as independent claims 21 and 40 recite.

As acknowledged by the Office Action, Wang is silent about forming an oxide layer "by oxidizing an upper surface of said source drain region using atomic oxygen," as independent claim 1 recites. Wang is also silent about forming a composite barrier layer "comprising an oxide layer formed by oxidizing upper surfaces of said source/drain regions using atomic oxygen," as independent claims 21 and 40 recite. Similarly, Mizuhara teaches *depositing* a silicon oxide film by Chemical Vapor Deposition (CVD) (col. 4, lines 52-54) and not "*oxidizing* an upper surface of said source/drain region using atomic oxygen," as recited in independent claim 1, or the formation of an oxide layer by "oxidizing upper surfaces of said source/drain regions using atomic oxygen," as independent claims 21 and 40 recite (emphasis added). In addition, Mizuhara teaches the deposition a silicon oxide layer over an aluminum alloy film or an organic SOG film (col. 4, lines 55-67; Col. 5; Figs. 2-4), and not "oxidizing *an upper surface of said source/drain region* using atomic oxygen" as independent claim 1 recites, or forming an oxide layer by "oxidizing upper surfaces of said source/drain regions using atomic oxygen," as independent claims 21 and 40 recite (emphasis added). For at least these reasons, the Office Action fails to establish a *prima facie* case of obviousness and withdrawal of the rejection of claims 1-8, 11, 13-24, 27, 29-43, 46 and 48-56 is respectfully requested.

Claims 9, 25 and 44 stand rejected under 35 U.S.C. § 103 as being unpatentable over Wang in view of Mizuhara as applied to claims 1-8, 11, 13-24, 27, 29-43, 46 and 48-56 above, and further in view of Lands et al. ("Lands")(U.S. Patent No. 3,571,914). This rejection is respectfully traversed.

As noted above, neither Wang nor Mizuhara, whether considered alone or in combination, teach or suggest the limitations of independent claims 1, 21 and 40. Similarly, Lands fails to teach or suggest forming an oxide layer "by oxidizing an upper surface of said source drain region using atomic oxygen," as independent claim 1 recites, much less forming a composite barrier layer "comprising an oxide layer formed by oxidizing upper surfaces of said source/drain regions using atomic oxygen," as

independent claims 21 and 40 recite. For at least these reasons, withdrawal of the rejection of claims 9, 25, and 44 is respectfully requested.

Claims 12, 28 and 47 stand rejected under 35 U.S.C. § 103 as being unpatentable over Wang in view of Mizuhara as applied to claims 1-8, 11, 13-24, 27, 29-43, 46, and 48-56 above, and further in view of Kirimura et al. ("Kirimura")(U.S. Patent No. 6,383,869 B1). This rejection is respectfully traversed.

Kirimura relates to "a thin film forming method and a thin film forming apparatus, in which a deposition gas and a radical material having different dissociation energies are used for forming a thin film." (Col. 2, lines 46-49).

None of Wang, Mizuhara and Kirimura, whether considered alone or in combination, teaches or suggests all limitations of independent claims 1, 21 and 40 for the reasons noted above. Claims 12, 28, and 47 are allowable for at least the reasons stated above for claims 1, 21 and 40 respectively. Withdrawal of the rejection of claims 12, 28, and 47 is respectfully requested.

Claims 10, 26, and 45 stand rejected under 35 U.S.C. § 103 as being unpatentable over Wang in view of Mizuhara as applied to claims 1-8, 11, 13-24, 27, 29-43, 46, and 48-56 above, and further in view of Asahina et al. ("Asahina")(U.S. Patent No. 6,326,287 B1). This rejection is respectfully traversed.

Asahina relates to a method for forming a "semiconductor device using, as a wiring material, a specific aluminum alloy which can be embedded in a through-hole without producing any void or wire breaking, and being highly resistant to electro-migration." (Col. 1, lines 37-41).

None of Wang, Mizuhara and Asahina, whether considered alone or in combination, teaches or suggests all limitations of independent claims 1, 21 and 40 for the reasons noted above. Claims 10, 26, and 45 are allowable for at least the reasons stated

above for claims 1, 21 and 40 respectively. Withdrawal of the rejection of claims 10, 26 and 45 is respectfully requested.

A marked-up version of the changes made to the specification by the current amendment is attached. The attached page is captioned **"Version with markings to show changes made to specification."**

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

By_____

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Version With Markings to Show Changes Made to Specification

On pages 3 and 4, please replace paragraph [0006] with the following:

[0006] The insulating layer 24 (Figure 2) is typically composed of a borophosphosilicate glass (BPSG) or a non-doped silicate glass (NSG), which is formed over the gate stacks 30 and the source/drain regions 40 by deposition, for example, and then undergoes a thermal treatment to facilitate the planarizing of the insulating material. Since the thermal treatment of the insulating layer 24 typically requires temperatures higher than 500°C, boron (B) and/or phosphorous (P) atoms from the BPSG insulating layer 24 migrate into the adjacent source/drain regions 40 and under the nitride spacers 32 in the LDD regions 42 during these high-temperature steps. Although the boron/phosphorous migration into the source/drain regions 40 occurs in limited regions, near or at a source/drain -BPSG interface 51 (Figure 2), this interface is degraded and the performance of the device affected. A major drawback posed by the migration of impurity boron/phosphorous atoms at the source/drain-BPSG interface 51 is the decrease in the "refresh time" of the DRAM device, and consequently an increase in the DRAM error rate. The "refresh time" of a DRAM cell is defined as the length of time over which the DRAM cell can retain a sufficient amount of charge for its intended data state to be determined by a sense amplifier circuit. Before this period of time expires, the DRAM cell must be reprogrammed or "refreshed" and, consequently, it is desirable that the refresh time between the refresh operations be as [along] long as possible.